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STRAY-INSENSITIVE, LEAKAGE-INDEPENDENT IMAGE SENSING WITH REDUCED SENSITIVITY TO DEVICE MISMATCH AND PARASITIC ROUTING CAPACITANCE

FIELD OF THE INVENTION

The invention relates generally to electronic circuitry and its operation and, more particularly, to the structure, control and operation of CMOS image sensing circuitry.

BACKGROUND OF THE INVENTION

CMOS image sensors are emerging as a viable alternative to CCD sensors due to the low power consumption and high integration capability of CMOS circuitry. However, CMOS imaging sensors also have various problems. One example is the so-called fixed-pattern-noise (FPN) caused by device mismatches and/or process nonuniformities. A mismatch occurs at each pixel site, and at each column read-out.

An example of a known CMOS imaging sensor is shown in FIGURE 9. The key blocks are: Pixel Block; Column Block; and Chip Output Block. The pixel Block (one for each pixel) includes the following: Photodiode PD; NMOS Transistor N1; and Switches RES and SEL. The Column Block (one for each column of Pixels) includes the following: Capacitors C1 and C2; PMOS Transistor P1; Switches CDS and COL; and Current sources IPIXEL and ICOL. The Chip Output Block (one for the whole chip) includes the following: PMOS Transistor P2; Switch CHIP; and Current Source ICHIP.

The operation of the Pixel Block is as follows: Node IN is connected to switch RES, the cathode of photofiode PD, and the gate of NMOS transistor N1. Initially switch RES is closed and the voltage on node IN is VRES. Then switch RES is opened. There will be a finite charge on node IN dependent on the voltage VRES, the capacitance of photodiode PD, and the gate capacitance of NMOS transistor N1. The photodiode current causes the charge on node IN to be discharged and the voltage on node IN decreases. Generally imagers have a fixed integration time or period. The voltage on node IN at the end of the integration period is referred to herein as VPD.

The voltage on node IN is read out using NMOS transistor N1 and Switch SEL, the Column Block circuit, and the Chip Output Block circuit.

FIGURE 10 summarizes the position of the switches during the Integration Period and the Pixel Readout, which enables the FPN to be suppressed.

During the Integration Period, RES and SEL are open. During the Pixel Readout, the following occurs.

Readout Step 1: RES and SEL are open, CDS, COL, and CHIP are closed to reset the Column and Chip Blocks. The voltage across C1 will be zero. The voltage across C2 is VP1gs, which is the gate to source voltage of PMOS transistor P1.

Readout Step 2: SEL is closed and COL is opened. The voltage across C1 becomes VPD – VN1gs (VN1gs=gate to source voltage of NMOS transistor N1). The voltage across C2 remains VP1gs.

Readout Step 3: CDS and CHIP are opened. The voltage across C1 remains VPD – VN1gs. The voltage across C2 remains VP1gs.

Readout Step 4: RES and COL are closed. The source voltage of N1 becomes VRES – VN1gs. The voltage across C1 remains VPD – VN1gs. Thus the gate voltage of P1 becomes (VRES – VN1gs) – (VPD – VN1gs) = VRES – VPD. The source voltage of P1 becomes (VRES – VPD) – VP1gs. The voltage across C2 remains VP1gs. Thus the gate voltage of P2 becomes (VRES – VPD) – VP1gs + VP1gs = VRES – VPD. The readout voltage OUT is

VRES – VPD + VP2gs where VP2gs is the gate to source voltage of PMOS transistor P2. PMOS transistor P2 is a common device used for the readout of all pixels.

Both VN1gs and VP1gs terms are canceled in this Sequential Correlated Double Sampling Technique. The N1 and P1 Vt terms, which are embedded in the VN1gs and VP1gs, are also canceled. Thus the effect of CMOS Vt mis-matches are suppressed with the above technique and the Fixed Pattern Noise is greatly reduced.

Readout Step 5: CHIP is closed. The readout voltage OUT equals VP2gs. The rest of the switches are opened. The pixel has been reset for the next Integration Period. The system is ready for the next pixel readout.

The above description is a readout operation for one pixel. During the Integration Period for one pixel, the Column Block and Chip Output Blocks are being used for Readout of other pixels.

Some problems with the CMOS imaging sensor of FIGURE 9 include the disadvantageous effect of parasitic routing capacitance caused by capacitors C2 (thousands of them in a complete pixel array) driving the transistor P2, and the fact that the capacitors are typically poly/n-well capacitors which disadvantageously tend to be stray-sensitive and also suffer from a leakage problem.

It is desirable in view of the foregoing to provide for CMOS image sensing that avoids the aforementioned problems associated with known CMOS imaging sensors.

According to the invention, a single capacitor can be used for both readout and reduction of device mismatches. Such dual-purpose use of a single capacitor is facilitated by a switching arrangement. The switching arrangement connects the capacitor to a low impedance node during charge storage, thereby advantageously providing the stored charge with a stray-insensitive, leakage independent characteristic. Also, the column readout line is driven by the low impedance node, thereby advantageously reducing parasitic routing capacitance.

BRIEF DESCRIPTION OF DRAWINGS

FIGURE 1 illustrates pertinent portions of exemplary embodiments of an imaging sensor according to the invention.

FIGURE 2 is a timing diagram which illustrates an example of the control and operation of the imaging sensor of FIGURE 1.

FIGURE 3 illustrates a reset state of the imaging sensor of FIGURE 1.

FIGURE 4 illustrates a read-out state of the imaging sensor of FIGURE 1.

FIGURE 5 illustrates pertinent portions of further exemplary embodiments of an imaging sensor according to the invention.

FIGURE 6 is a timing diagram which illustrates exemplary signals which can be used to control operations of the imaging sensor of FIGURE 5.

FIGURE 7 illustrates a sampling state of the imaging sensor of FIGURE 5.

FIGURE 8 illustrates a read-out state of the imaging sensor of FIGURE 5.

FIGURE 9 and 10 illustrate a known CMOS imaging sensor arrangement.

DETAILED DESCRIPTION

FIGURE 1 illustrates pertinent portions of exemplary embodiments of a CMOS imaging sensor according to the invention. The imaging sensor of FIGURE 1 includes a pixel circuit 11 and a column read-out circuit 13. The imaging sensor of FIGURE 1 includes a plurality of circuit nodes designated as n1, n2, n3, n4, n5, n6 and n7. The column read-out circuit 13 includes a poly/n-well capacitor C coupled between nodes n5 and n6, and a buffer coupled between nodes n4 and n7. The pixel circuit 11 includes a photodiode PD as is conventionally used in CMOS imaging sensors.

The imaging sensor of FIGURE 1 further includes a switching arrangement including a plurality of switches for selectively interconnecting various nodes in the imaging sensor. Each switch of the switching arrangement is controlled by one of a plurality of control signals designated in FIGURE 1 as $\Phi 1$, $\Phi 2$, $\Phi 3$, $\Phi 4$ and $\Phi 5$. These control signals are also illustrated in the timing diagram of FIGURE 2. The timing diagram of FIGURE 2, taken in conjunction with FIGURES 1, 3 and 4, illustrates an example of the control and operation of the imaging sensor of FIGURE 1.

Referring now to FIGURES 1-3, when $\Phi 1$ (reset), $\Phi 3$ (row select) and $\Phi 4$ (hold) are high in FIGURE 2, the corresponding switches in FIGURE 1 are closed, and the remaining switches

controlled by Φ2 and Φ5 are open. Thus, at this time, the imaging sensor of FIGURE 1 has the circuit configuration illustrated in FIGURE 3. At this time, the voltage across the capacitor C is:

$$\Delta V_c = V_{ref} - (V_{ref} - V_{gs,M} + V_{off,M} + V_{off,buf})$$

where $V_{gs,M}$ represents the gate-source voltage of the NMOS driver M, $V_{off,M}$ represents the DC offset of the driver M, and $V_{off,buf}$ represents the DC offset of the buffer.

When Φ4 (hold) goes low and Φ5 (column select) goes high after exposure, the sensor of FIGURE 1 assumes the circuit configuration illustrated in FIGURE 4. In this configuration, the output voltage is given by:

$$\begin{aligned} V_{out} &= V_{ph} - V_{gs,M} + V_{off,M} + V_{off,buf} + \Delta V_c \\ &= V_{ph} - V_{gs,M} + V_{off,M} + V_{off,buf} + V_{ref} - (V_{ref} - V_{gs,M} + V_{off,M} + V_{off,buf}) \\ &= V_{ph} \end{aligned}$$

where V_{ph} is the voltage across the photodiode PD.

It can be seen from the foregoing that all of the mismatch offsets are stored in the capacitor C during the reset phase, and are then cancelled out in the read-out phase. That is, the operation illustrated in FIGURES 1-4 uses the reset phase, as controlled by $\Phi 1$, to store the mismatch information into the capacitor, and the mismatch information is then cancelled out during the read-out phase controlled by $\Phi 4$ and $\Phi 5$. This means that the operation described above with respect to FIGURES 1-4 can read-out only one row of the image sensor array at one exposure time. Accordingly, in applications that have a particularly long exposure time, the embodiments of FIGURES 1-4 might not be able to read out the whole image sensor array as quickly as desired.

FIGURE 5 illustrates pertinent portions of exemplary embodiments of a CMOS imaging sensor according to the invention which can provide faster operation than the imaging sensor of FIGURE 1. The image sensor of FIGURE 5 includes generally the same circuit elements as FIGURE 1, but has a differently designed arrangement of switches for controlling interconnection of the circuit elements. The sensor of FIGURE 5 includes nodes n11, n21, n31 and n41, and each of the switches in the FIGURE 5 switching arrangement is controlled by one of a plurality of control signals $\Phi 11$, $\Phi 21$, $\Phi 31$ and $\Phi 41$. The image sensor of FIGURE 5 also utilizes two voltage references, V_{ref1} and V_{ref2}, to increase the output signal swing range.

FIGURE 6 is a timing diagram which illustrates the signals Φ11, Φ21, Φ31 and Φ41 which control the image sensor of FIGURE 5. As shown in FIGURE 6, the image signal is read-out by operation of Φ41 (column select) during the second pulse of Φ11 (reset).

Referring now to FIGURES 5 and 6, during the sampling phase, when Φ21 (sample) and Φ31 (row select) both go high, the image sensor of FIGURE 5 assumes the circuit configuration illustrated by FIGURE 7. In FIGURE 7, the voltage across capacitor C is given by:

$$\Delta V_c = V_{ref2} - (V_{ph} - V_{gs,M} + V_{off,M} + V_{off,buf}).$$

During the read-out phase, with Φ11, Φ31 and Φ41 all high, the image sensor of FIGURE 5 assumes the circuit configuration illustrated in FIGURE 8. In this configuration, the output voltage is given by:

$$V_{out} = V_{ref1} - V_{gs,M} + V_{off,M} + \Delta V_c + V_{off,buf}$$
$$= V_{ref1} + V_{ref2} - V_{ph}.$$

Again, the offset mismatch does not appear in the output voltage V_{out}, which is read-out during the reset phase. Therefore, different rows of an image sensor array can partly share the exposure time illustrated in FIGURE 6.

In view of the foregoing discussion, it will be evident to workers in the art that the imaging sensor embodiments of FIGURES 1-8 are: insensitive to parasitic routing capacitance because the output nodes n7 and n41 are low-impedance nodes; low power sensors because they provide a true column-parallel read-out; leakage and stray insensitive although using a poly/n-well capacitor, because the n-well is connected to a low-impedance node during charge storage. Moreover, and assuming that the capacitors C within a given sensor array are well matched, charge-injection and clock-feedthrough do not present a problem because they are common-mode signals to all pixels of the array.

Although exemplary embodiments of the invention are described above in detail, this does not limit the scope of the invention, which can be practiced in a variety of embodiments.